GPS Disciplined Frequency Reference - Traps for the Young and not so Young

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A paper presented to the GippsTech Microwave Conference 2019.

This presentation aims to summarize my experimentation in getting to GPS disciplined frequency generator solutions with measured results that satisfy me and to explain the traps identified when assisting others over the last year or more.

A copy of the PowerPoint presentation and a recording of the presentation by GippsTech are available. If a search does not find these, please email <mycallsign> at WIA.org.au

Introduction

The 'flavour of the month' seems to be GPS locking of radio frequency. In some circles, the fact that one can claim "GPS locked" appears to be more important than being confident of the frequency accuracy or stability of the radio.

With the lack of sunspots, and the search for higher and higher frequency capability, weak signal technology and stable / on frequency generation of local oscillators for DC to daylight transverters has become the focus of the hobby particularly for VHF/UHF enthusiasts.

My interest has been focussed below an upper limit of 1 GHz, a self-imposed glass ceiling as the limit of my interests. Maybe it is the impact the number of stations that call off frequency in competitions or regular skeds such as 23 on 23rd and the criticism of my signal during EME WSJT QSOs that developed a view that we were not doing frequency locking well.

As a retired and senior technologist, I get exposed to projects of many other amateur radio operators. This has led me to the view that many of the designs being pedalled to our community are inadequate and that there is much "wrong drum" published.

I am lucky enough to have reasonable test gear, and to have career experience in hardware and embedded microprocessor design.

This presentation aims to summarize my experimentation in getting to GPS disciplined frequency generator solutions with measured results that satisfy me and to explain the traps identified when assisting others over the last year or more.

This subject of frequency locking, particularly by using a 10MHz "Standard" is not new. Using GPS receivers and microprocessors to discipline references has been extended over the years. I recognise I may be presenting solutions published before my examination of this subject.

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Why Lock Frequency?

In my activities, two reasons for locked frequency are:

Frequency accuracy. So the other station can find me when I call on sked, so that I am on calling frequency for general calls, and when operating in digital modes (e.g. WSPR) to operate in the band segment, to be on a specific frequency, and to avoid clashing with other stations. It is also important to be correct in reverse beacon reporting.

My estimate of required accuracy is within 100 Hz up to 1296MHz.

Frequency stability. QSOs are made more difficult where transmissions drift or jump. In digital modes, the software depends on accurate time and stable frequency to provide the best chance of being decoded. It is also important for my decoding of other's digital transmissions.

It is preferable that stability is better than 10 Hz up to 1296 MHz.

Ideally these accuracy and stability tolerances are held for all operating conditions: voltage, ambient temperature, power output, SWR, radio temperature, cooling fan on or off.

Frequency Generation

Direct frequency generation has been the norm. That is the local oscillator or transmitter frequency has been generated on the operating frequency. Crystals or crystals and multiplier providing high stability with acceptable accuracy. Particularly with the emergence of solid-state designs variable frequency oscillators (VCOs) developed to be stable enough for most modes including SSB. Phase locked loop (PLL) designs improve the performance of the frequency generation. PLLs depend on a reference typically generated by a crystal. As the PLL frequency may be many times that of the crystal, improvements in the stability and accuracy of the reference generator were sought. In its simplest form this was temperature control of crystals cut for high stability at a specific temperature well above ambient.

The frequency accuracy problem meant calibration against a standard such as WWW frequency broadcast.

As higher stability was sought typically as the operating frequencies moved into the VHF, UHF and higher band, better references were sought to lock the frequencies in the amateur station. Many of these references brought inherent high frequency accuracy as well.

10MHz has become the standard for station frequency reference.

The holy grail of 10MHz standards has long been caesium or rubidium laboratory frequency references. Commercial GPS disciplined frequency reference have recently claimed a place in this role at a lower price with generally less complex setup and possibly greater reliability.

Oven controlled crystal oscillators OCXOs have become more available and higher performance with their mass production for communication network equipment. Many high specification types are available in the surplus market.

Volume production of miniature temperature compensated crystal oscillators (TCXO) means the options for high performance at low prices (and small size) are increasing.

The latter two require manual calibration or automatic disciplining by other frequency or time standards (GPS, caesium / rubidium).

The topology adopted for most modern transceivers is PLL(s) for frequency conversion and programable logic array (PLA) for modulation / demodulation of a range of operating modes. As the PLAs and microprocessors have developed Software Defined Radio (SDR) have seen the base (intermediate frequencies IF) increase. Highly stable and accurate frequencies are still required for the initial conversion process in these SDRs. In most cases the PLL fed with a frequency reference is a critical block of these designs.

Digital Clock Generator

The technologies emerging from cellular phone development provide more stable and accurate frequency generation than traditional methods such as multiplied overtone crystal oscillators. While the designs are inherently more complex, there are many sources of economic integrated solutions available from local and overseas suppliers.

Many of these designs use microprocessors to setup and control the frequency (clock generator). These too are supported by many on-line suppliers / developer groups so that with some application, many experimenters can customize a design to their requirements.
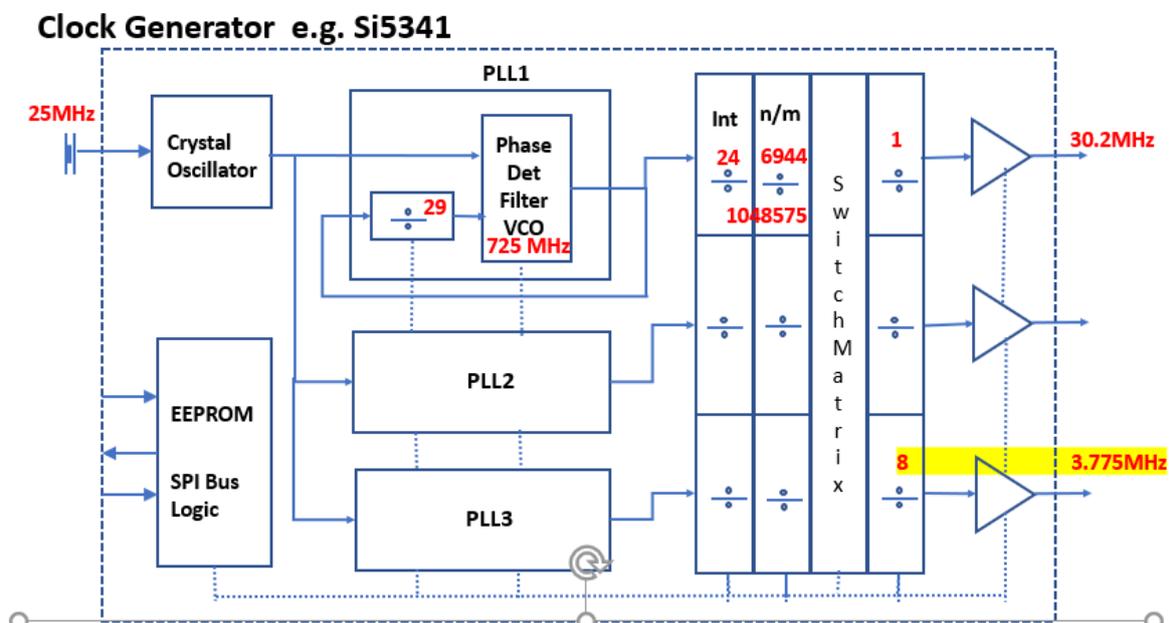
While the topology and frequency range of the frequency generator integrated circuits varies widely, the building blocks are generally common. The block diagram of the popular Si5341 is shown below. A frequency range of 8KHz to 160MHz is typical while frequencies up to 712 MHz are possible with this part. Other parts provide frequency generation to microwave (e.g. 4.4GHz, 13.4GHz max). Up to ten independent frequencies may be generated in some types.

The annotations on the block diagram show PLL1 phased locked to a 25MHz crystal by using a divide by 29 from the PLL output to the phase detector. The output of PLL1 may then be selected to a divider chain and output stage. The initial divider consists of a integer divide of 24 followed by a fractional divide of 0.00662232076866 (6944 nominator over 1048575 denominator). A final divide of 1 provides 30.2MHz to the output stage.

The configuration of the PLL, dividers and switching matrix is provided by SPI communications from a microprocessor.

The example above also shows an output divide of 8 providing 3.775MHz for frequency counting by the microprocessor.

GPS Disciplined Frequency Generation

The digital clock generator may be disciplined / locked to frequency by measuring its frequency over the period of the 1 PPS output of a GPS receiver.

The accuracy of the 1 PPS output of a GPS receiver locked onto 3 or more satellites is better than sub-microsecond (99% error less than 60nS <= 0.06 ppm).
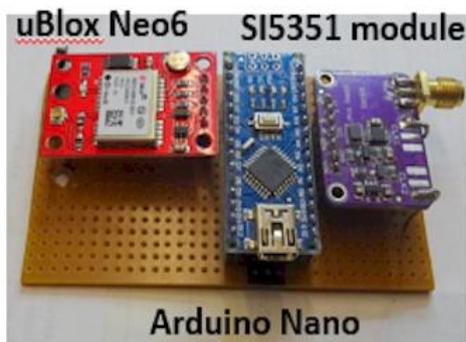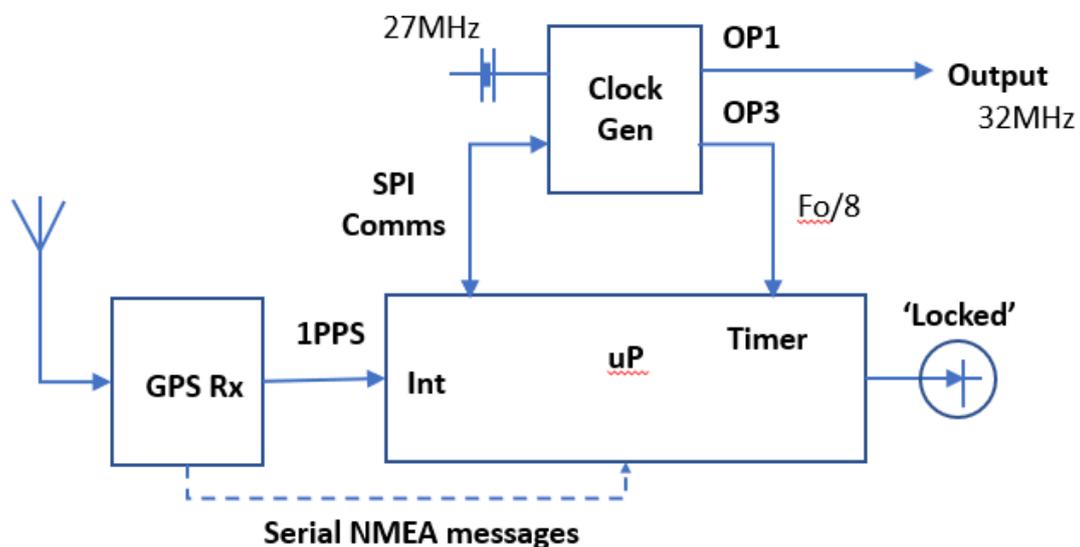
GPS Disciplined Frequency Reference - Traps for the Young and not so Young

Fundamental operation involves configuring the clock generator to frequency for the optimum PLL frequency and divide ratios and for the reference crystal frequency. The output frequency is counted using interrupts from the 1 PPS signal from the GPS receiver. The locked status of the 1 PPS may be indicated by the 1 PPS availability or by status flags in serial NMEA messages output from the GPS receiver.

Limitations on the maximum count rate of the microprocessor timer means the output frequency may be divided before passing to the microprocessor. The error in frequency either at this sub-frequency or over multiple 1 PPS periods may be applied to the dividers in the clock generator to correct / discipline the oscillator to frequency. The correction logic may average the error or calculate a rolling error over extended periods before applying using a proportional-integral-derivative (PID) or fuzzy logic control loop.

Other errors inherent in this configuration include:

- Granularity due to the digital divider   +- 1Hz for Si 5351 at 30 MHz Far more at 4.4 or 13.4 GHz
- 1PPS interrupt latency   1us latency produces 4 Hz error
- Correction Latency   drift of 10 Hz in 10 sec produces 12Hz error
- Frequency Counter Resolution   with counter at $1/8^{th}$ output frequency, 7 Hz error

Note errors are additive e.g. Total error > 20Hz at 30.2 MHz approximately 1 ppm. When used as a reference for a 1296 MHz transceiver the error is 850Hz

The advantages of this configuration of GPS disciplined Frequency Generator include:

- Simple low-cost hardware
- Frequency ranges 200kHz to 200MHz; 138MHz to 4.4 GHz; 138MHz to 13.4 MHz
- Low cost crystal frequency source for PLL

The disadvantages include:

- Frequency accuracy limited by:
    - Maximum Frequency of microprocessor as counter
    - GPS and microprocessor interrupt timing jitter
    - Frequency Count resolution
    - Granularity of frequency generator phase-locked-loop and dividers
- Frequency Stability limited by:
    - Latency in frequency count
    - Latency in applying corrections
    - Crystal affected by ambient temperature

Performance of a GPS disciplined frequency generator at 30.2 MHz were recorded for an

- Arduino Nano 3V 8Mhz
- Neo6 GPS receiver providing 1 PPS
- QRP Labs 27 MHz Si5351 OCXO
- Frequency measured at 3.775 MHz ($1/8^{th}$ 30.2 MHz)
- Frequency averaged over 8 seconds and applied at 10th second
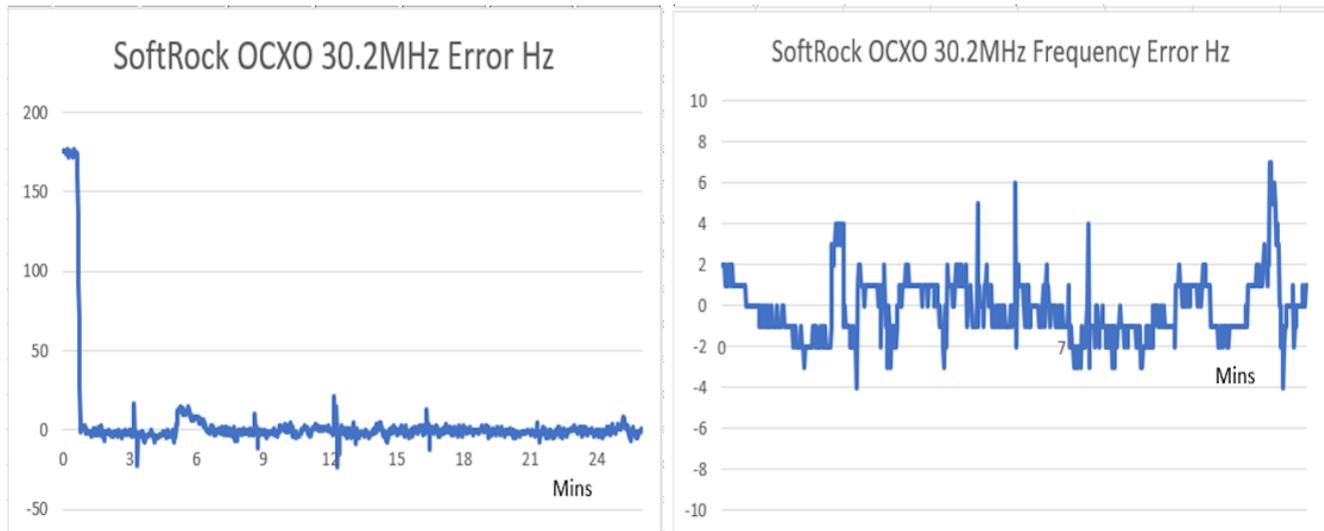
When examining the errors contributing to this poor performance, the following is noted:

- Granularity can't be avoided. The finest step size can be achieved by selecting the highest PLL design frequency and by carefully selecting the integer and fractional divide ratios.
- Minimising interrupt latency involves selecting a microprocessor with the highest possible clock frequency; keep the code structure simple and avoid blocking functions; keep the interrupt service code simple (only essential actions within ISR); and count the output of the frequency generator over multiple 1PPS periods.
- Best correction latency is achieved with crystal frequency selection to minimise drift; providing an insulated environment for the crystal or provide a heated environment or use a oven controlled crystal oscillator.
- Factors in minimising frequency counter errors include:
  - select a microprocess or async external input to timer / counter; avoid resetting timer and overflow counts;
  - count frequency over multiple 1PPS periods (e.g. count eight periods if one eighth generated frequency);
  - adopt coarse then fine correction strategy (Course correction 1Hz at 8 second intervals then fine 0.1Hz at 80 second periods); and
  - average the count over multiple periods or use a rolling average of the count error.

Other factors identified during software development and experiments include:

- Apply frequency correction using Fuzzy logic not process-intense PID control logic;
- Consider count certainty in selecting the dead band in the correction algorithm;
- Avoid compiled code structures known to be unfriendly to embedded microprocessors (e.g. variable arrays, select case, indexed for loops,);
- Use specific frequency generator interface code not processor intense general case library structures;
- Use device specific communications protocols which update only the essential parameters;
- Customise constants for specific hardware (e.g. don't use nominal crystal frequency, measure the frequency under exact operating conditions and use that close match – immediate improvement in performance).

After more than a thousand hours of research, hardware and software development, testing and modification later lead to a design which minimised all errors. The result was stability equal to the granularity of a Si5351 frequency generator (e.g. 1Hz at 30 MHz).
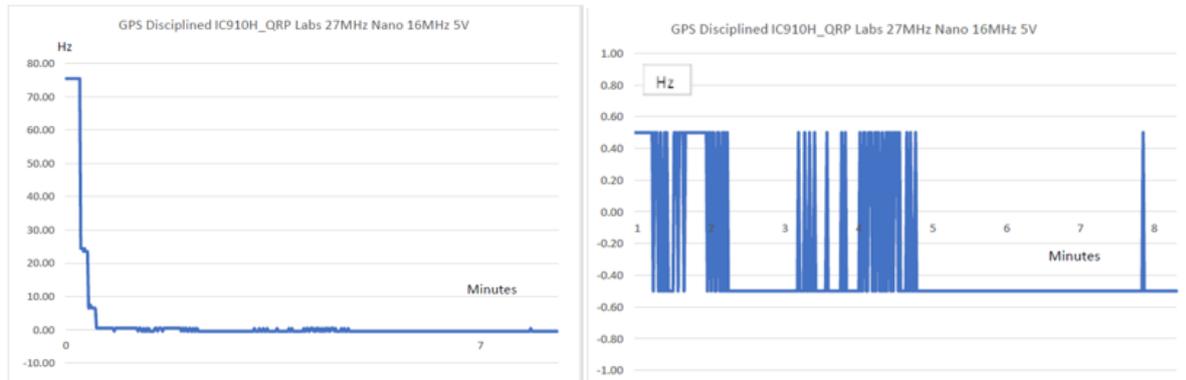

This result, +- 0.5 Hz or 1.6 ppb was achieved with an Arduino Nano 5V 16MHz; a Neo6 GPS receiver 1PPS; and a QRP Labs 27MHz OCXO in a Si5351 synthesiser. The frequency was counted at 7.75MHz over a 8 second period. After initial correction, a rolling error calculated over 80 seconds was applied every 100 seconds.

The question however remains. "Nearly perfect but is it good enough ????"

An Alternative Approach – 10MHz locked PLL or Reference Generator

The errors due to quantization are avoided if a highly accurate and stable 10 MHz source is used as reference to the digital reference generator or phase locked loop in the radio. In these cases, the divide ratio is fixed and the radio reference frequency doesn't need to be measured. Thus another group of errors are avoided.
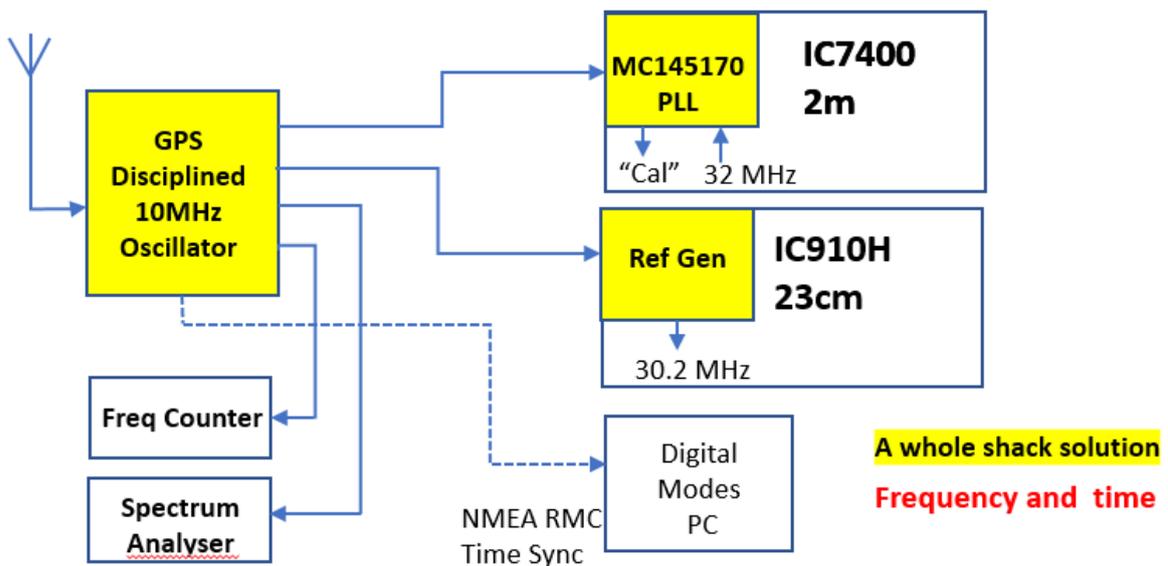
A range of 10 MHz frequency references are available (see the next section). Even when GPS disciplined reference generator in the previous section is used to provide a 10MHz reference, the frequency locking results are more than satisfactory (better than 1 ppb) for local oscillators up to microwave bands.

This block diagram shows the relationship between the system elements. The 10MHz reference may be used to lock the radios, as well as the test equipment, in the shack.

The time reference usually available from the 10MHz frequency reference may then provide time synchronisation for the shack computer and digital mode applications.

There are plenty of examples of the 10MHz reference locked phase locked loop (e.g. MC145170) in application notes and amateur radio projects.

The use of digital clock / frequency generators is also widely published. The following example uses a Si5351 setup by an ATMega328 microprocessor (basically the same hardware as the GPS disciplined reference generator but 10 MHz frequency locked).

The microprocessor functions are minimised to initialise the clock generator, detect the availability of the 10MHz standard, enable the output of the clock generator, and switching of the supply to the radio's internal frequency reference.

This hardware solution may be applied to most modern radio designs which use an internal frequency reference for the local oscillators including software defined radios.
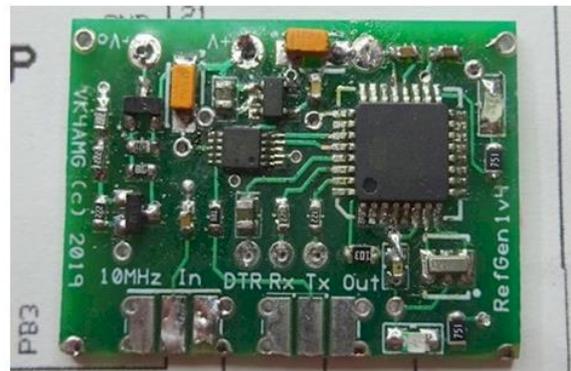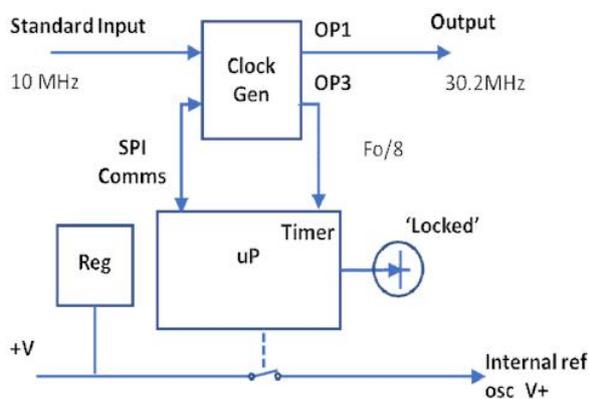
Options for 10MHz Reference

Crystals[*]

The crystal has been the stable frequency reference for decades. The modern SMD component may be as small as 3 x 1 mm. Frequency accuracy for a low-cost crystal may be 20 ppm (200 Hz at 10Mhz) with similar stability over a temperature range of 0 to 60 deg C. Fundamental frequencies are limited to HF but overtone types are available to provide up to 200MHz. Accuracy and stability of overtone types are reduced by the overtone factor. Overtone crystals are not suitable for oven-controlled applications. **TCXO**[*]

 The crystal may be included in a 2 x 1.6mm oscillator package. The latter may include circuits for temperature compensation of the oscillator. That is applying compensation for the inherent temperature characteristic of the crystal. A low cost TCXO may provide +-2ppm stability over 0 to 60 deg C with a similar frequency accuracy and an ageing less than 1 ppm.   Phase noise from these devices are typically -115dBc at 10Hz.

NOTE: [*] These lower cost options (crystals and TCXO) require manual calibration or GPS Disciplining for high frequency accuracy. They must be insulated from the environment and temperature controlled for good short-term accuracy and stability. Temperature compensation is not enough for most applications. Lag in compensation may otherwise degrade performance.

OCXO

Prior to the GPS era, crystals with integrated oscillators were packaged in temperature-controlled ovens. These crystals were cut to have a flat frequency vs temperature characteristic around 60 deg C. These TCXOs became the reference for many telecommunications systems. The frequency accuracy, unadjusted, is better than 1ppm (10Hz at 10Mhz). Frequency stability is typically 10 ppb (0.01Hz at 10MHz)) over a temperature range of -30 to 70 deg C. Phase noise is typically -115dBc at 10kHz.

These oscillators still suffer ageing of up to -+300 ppb over 10 years. many of these oscillators are voltage adjustable to calibrate the oscillator or to compensate for age changes.

Various techniques for disciplining / correcting TCXOs have been applied. These oscillators are suitable for GPS discipline but are excellent even with occasional calibration.

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GPS Frequency Generation

Many low-cost GPS receivers may be configured to output a specific frequency as an alternative to a 1PPS. A uBlox NEO6 was configured for 10 MHz but the output showed significant jitter. This frequency may be suitable as a reference for a PLL with frequency smoothing. Range of frequencies are limited to HF.

Professional GPS Receivers

Many Trimble, Garmin, etc professional receivers (e.g. Thunderbolt) can provide a highly accurate and stable frequency reference. As well as the expected cost ($3000 plus new), many of these units are complex to configure.

 The frequency accuracy and stability are excellent (better than 1×10^{-12}). Phase noise is similar or better than the crystal oscillator. Typically limited to providing station 10MHz frequency reference.

Caesium / Rubidium Reference

These laboratory standards are out of the reach of most amateurs (upwards of $12,000). Used units are available in surplus market for around $500. Caesium tubes, the core of the Caesium Unit have limited life and are expensive to replace (more than the price of most used units). Frequency accuracy and stability better than 0.001 ppb.

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| Type	Accuracy	Stability / Day	Price	
Rubidium Caesium Frequency Standard	0.001 ppb	0.001 ppb	$500++	Used
GPS Disciplined Oscillator	0.01 ppb	0.001 ppb		
e.g.Trimble Thunderbolt			$500	Used
G7TBL GPDDO			$300	New
Oven Controlled Crystal Oscillator	Not calibrated			
e.g. Morion MV89		0.5 ppb	$ 50	Used
IsoTemp-131			$ 50	Used
Temperature Compensated Crystal Oscillator	Not calibrated			
e.g. SiTime 5356AI		0.1 ppm	$ 75	New
IQT LF TVX009900		0.2 ppm	$ 20	New
CTS 580L100X2		0.25 ppm	$ 20	New
Voltage Controlled Crystal Oscillator	Not calibrated	25 ppm	$20	New

NOTE: ppb = parts per billion = 1 per 10^9 ppm = parts per million = 1 per 10^6

GPS Disciplined Frequency Reference - Traps for the Young and not so Young

GPS Disciplined 10MHz Oven Controlled Oscillator

Lower cost options may be manually calibrated or GPS Disciplined. This design takes the characteristics of an IsoTemp-131 TCXO and disciplines its frequency accurately using the timing signal from a GPS Receiver.
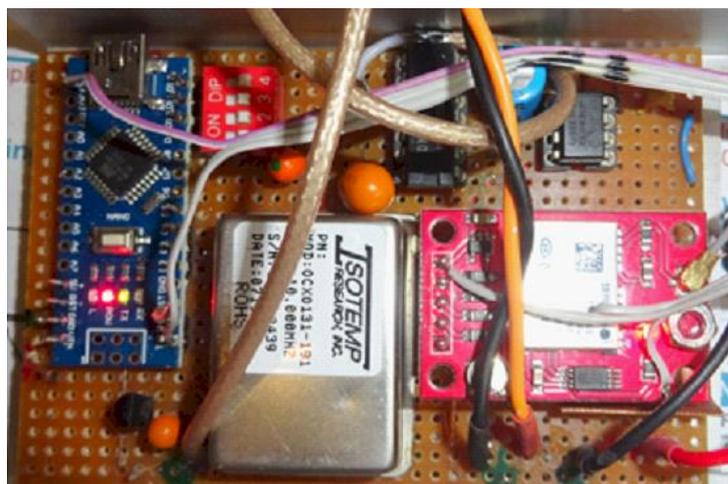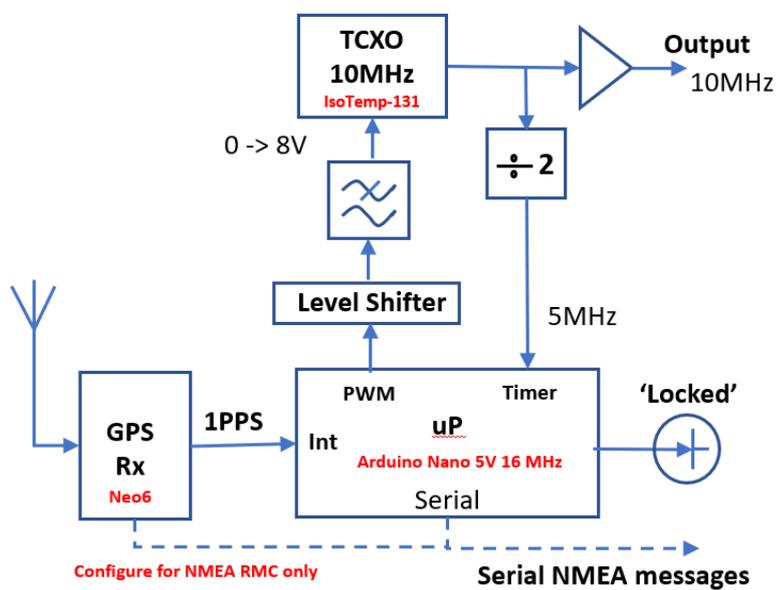
The IsoTemp-131 voltage-controlled crystal oscillator (VCXO) provides:

- Excellent accuracy +- 20 ppb uncorrected
- Excellent stability +- 0.5 ppb per day
- Fine pulling range +- 4 ppm
- Control range 0-8 Vdc (within DAC or PWM level-shifted)
- Supply is 12 V at less than 12 W (< 1.5 W quiescent)
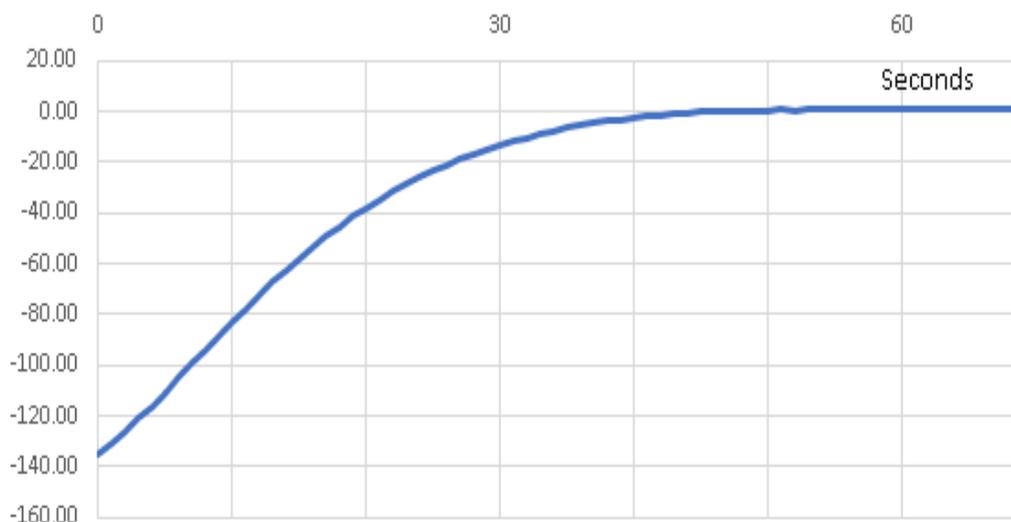- Low phase noise

Phase Noise @ 10 MHz		
@ 10 Hz	-120	
@ 100 Hz	-135	
@ 1 kHz	-150	dBc
@ 10 kHz	-150	
@ 100 kHz	-150	

When disciplined the accuracy is < +- 2ppb.


Freq Error OCXO-131 after Warm-Up(Hz)
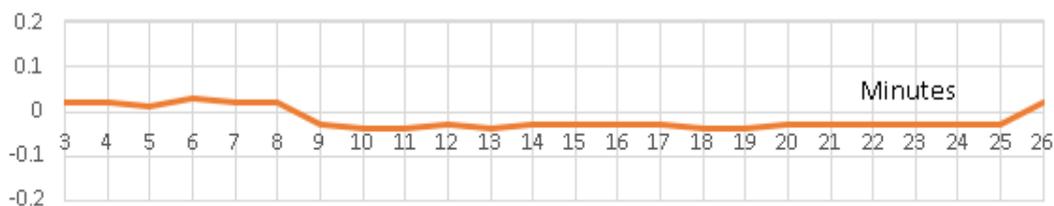
Freq Error OCXO-131 from Cold (Hz)

Once the correction is characterised, fast turn-on (less than 10 seconds) can be achieved by using EEPROM stored parameters as the starting condition. The IsoTemp-131 was found to be so stable that little or no discipline is necessary on subsequent power-up. The device may be confidently used without discipline. Occasional calibration for frequency accuracy is likely enough for most applications.

Another popular OCXO is the Morion MV89A which is readily available in surplus markets. In comparison with the IsoTemp-131, the MV89 consumes more power (20 W, 4W quiescent), takes much longer to warm-up (15 to 20 minutes), and has a wider pulling range (25 ppm - more care required in applying corrections). Stability is better at <0.0002 ppb with a sine wave output at +7 dBm.

Morion MX89 Error Hz from Cold

Morion MX89 Error Hz after Warmup
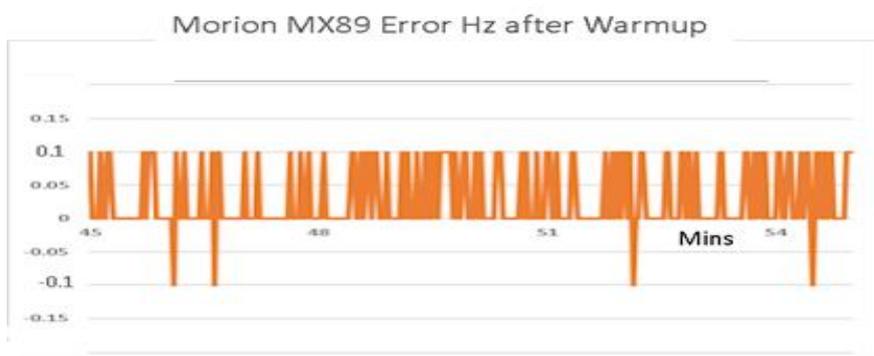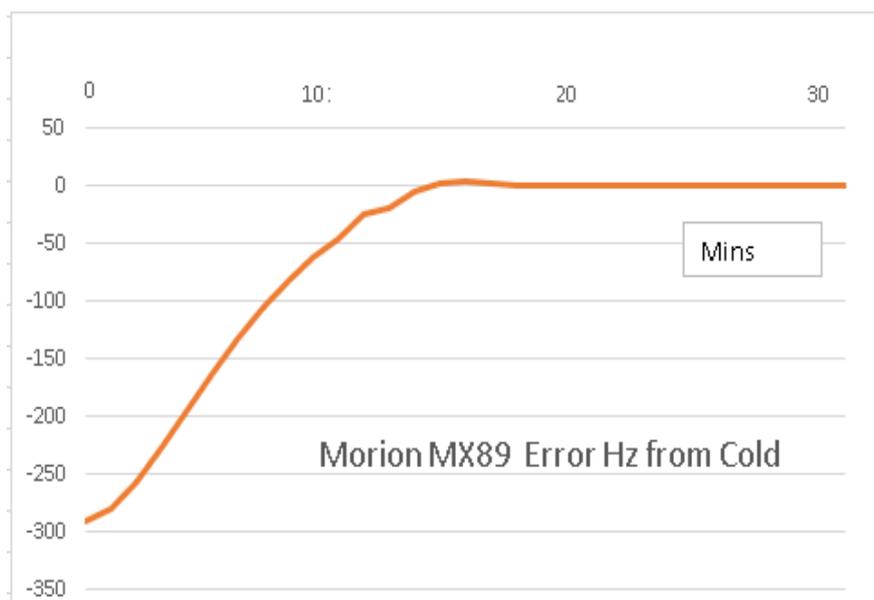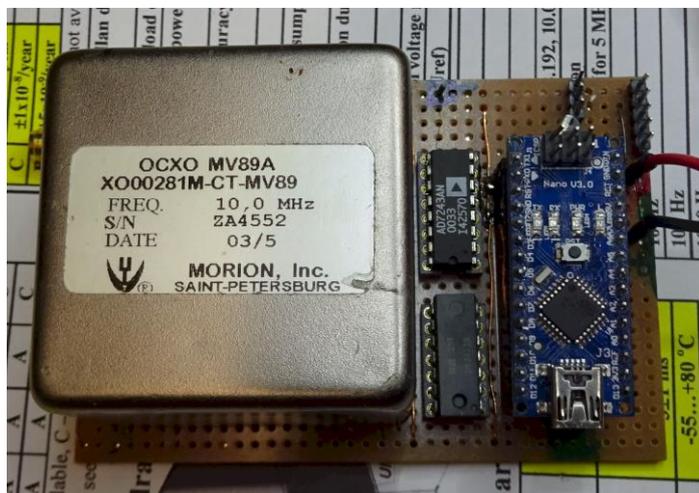
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Frequency Generator using a GPS Disciplined Voltage Controlled Crystal Oscillator

This approach avoids the granularity issues of the digital clock generator. The microprocessor is still required to count the output frequency but instead of adjusting the divide ratio in the clock generator, the frequency of a voltage-controlled crystal oscillator VCXO is adjusted.

The hardware used in this solution is QRP Labs ® "Improved Prog Rock" Si5351 module kit and their QRP shield for an Arduino Uno processor.

The hardware used a 27MHz ASVV VCXO mounted on the QRP shield. The PWM output of the Arduino Uno is filtered by two state RC filter at 27 and 270 ms time constant. By combining 1/10th of this DC control signal with a 3.3 V refence signal, +- 1.5 kHz control range is achieved with 2^{16}-1 steps (1ppb).

The same limitations apply to the frequency counting and correction described in the first section.
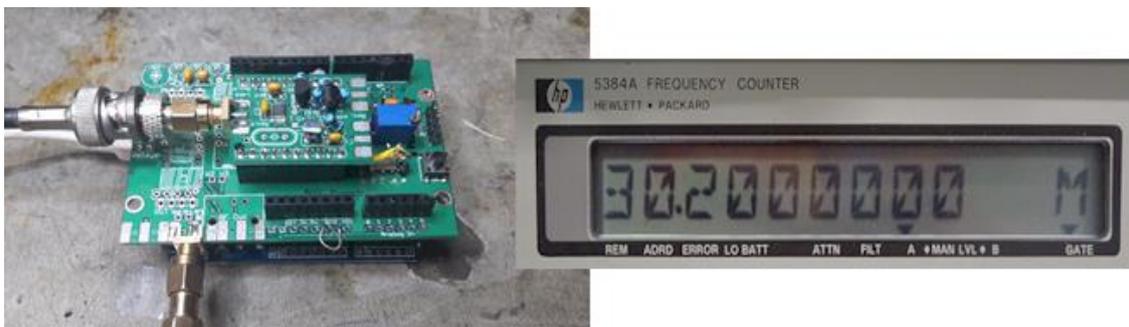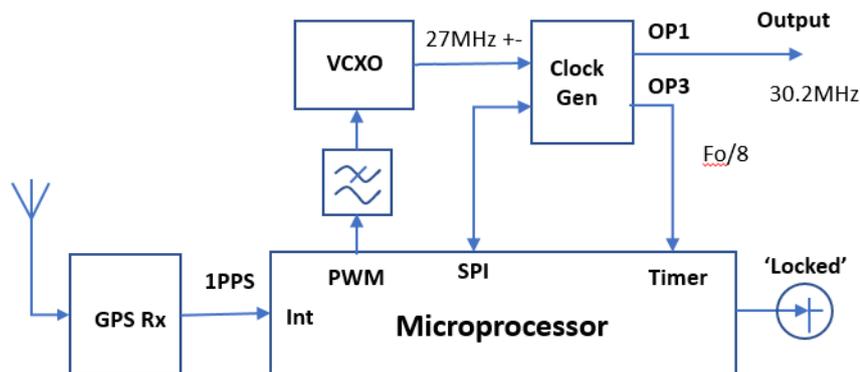
The design strategy includes:

- Si5351 OP3 provided <5MHz to Timer 1 for Counting and PWM generation
- 16 MHz Arduino Uno AT328n Timer measures 5MHz with excellent repeatability
- Eight successive frequency counts are added to calculate frequency error
- Rolling average of error is calculated over eight further seconds
- This error is applied by fuzzy logic to PWM duty cycle
- Thirty second settling period allowed between corrections
- Less than five minutes is required to settle output within 10Hz
- Another 5 to 10 minutes settles the output frequency to better than 1 Hz accuracy

Note the ASVV VCXO is affected (typically +-25ppm) by ambient temperature changes. This design requires VCXO temperature, frequency counting and correction errors to be considered and controlled.

QRP Labs provide as part of their WSPR beacon project a oven controlled crystal oscillator version of the Si 5351 synthesiser module. This module aims to improve on the "Prog Rock" module by providing temperature-controlled oven, isolate load from the crystal oscillator, and improve power supply regulation and isolation.

1ppm stability over a 2-minute WSPR transmission is claimed. Frequency discipline using GPQ 1PPS may be applied for long term stability.

I have not attempted to measure or compare the QRP Labs modules for frequency accuracy. The comments on potential errors in the first section of this paper are applicable.

Combining the Improved "Prog Rock with QRP Labs OCXO should provide 1 PPB accuracy and stability.

Conclusions

- Modern digital modes require high frequency accuracy and stability as well as accurate timing.
- Digital Frequency Generators have quantisation limitations which cannot be overcome.
- Combination of 10MHz "Standard" feeding PLL or Frequency Generator provides good result.
- GPS disciplined VCXO may be combined with digital Frequency Generator to provide a good result.
- 10MHz "Standard" or VCXO with Freq Gen must be insulated from temperature changes.

While my experimentation shows a GPS Disciplined digital clock generator can provide excellent stability and accuracy, the quantisation errors inherent in the clock generator means a suitable solution for all applications is not achieved. This topology can however provide a suitable 10MHz frequency reference.

The well proven approach of distributing 10MHz reference to synthesisers has been revisited and shown to provide excellent solution. Several economic sources of 10MHz reference signal have been identified. The IsoTemp-131 and Morion MV89 VCXO provide excellent stability and when GPS disciplined provide excellent frequency accuracy as well.